APPLICATION NOTE

TDA9964/52
IMAGING FRONT END BOARD CAMERA
CAMDEMO 9952/9964

AN00011

Philips
Semiconductors

PHILIPS

Summary

This application note describes an Interface Font End Board formed from a TDA9964/52 Philips imaging integrated circuit and a ¼ " mid resolution Sharp CCD sensor and its companion circuits.

The front-end board has been developed in such a way that it can be easily connected to an evaluation board of the Philips DSP family.

Associated with a sister DSP board built around the SAA8112 this IFE board gives an example of basic video camera application.

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APPLICATION NOTE

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IMAGING FRONT END BOARD CAMERA
CAMDEMO 9964/52

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1 IC FRONT END TDA9964/52 DESCRIPTION

1.1 Functions included in the front-end

The TDA9964 is a 3V, 12 bit analogue to digital interface for CCD cameras. This device includes in a LQFP 48 package:
The TDA9952 is a 3V, 10 bit analogue to digital interface for CCD cameras. This device includes in a LQFP 48 package:

. a correlated double sampling circuit (CDS)
. CDS programmable bandwidth
. an amplifier with a variable gain digitally controlled (AGC)
. AGC programmable bandwidth
. an +6db amplifier for analog iris control
. a low power 12 bit Analog to Digital Converter for TDA9964, 10 bit for TDA9952
. necessary video clamp circuits
. integrated reference voltage regulator
. serial interface function for programming internal registers (SRI)
. circuits for internal clocks generators
. and additional 8 bit Digital Analog Converter which is available for extra external control function
. programmable standby mode of main function facilities

The TDA9952 has a 20 MHz maximum clock frequency.
The TDA9964 has a 40 MHz maximum clock frequency.

2 FUNCTIONAL DESCRIPTION

2.1 General description

The TDA9964/52 are a low power, low voltage circuits which are able to operate under 2.7 volts to 3.6 volts of VCC supply voltage.

Analog and digital supplies of this IC have several separated pins VCCA and VCCD and VCCO. Therefore special care must be taken when an application board is designed in order to avoid any external disturbing effect when using a non correct filtering circuit around these VCC lines see chapter 5.

The TDA9964/52 need 11 dedicated logic signals to work in its basic configuration.

- 1 clock signal at the pixel frequency CLK;
- 2 sampling signals SHP and SHD;
- 4 clamp signals CLPOB, CLPDM, CLPADC and PBK;
- 4 connections concerning the serial bus SDATA ,SCLK, SEN and VSYNC.

All these digital inputs, as standby inputs STBY and enable not EO(N) are logic level TTL compatible.
In addition in this version the outputs are CMOS level compatible. That is why no adaptation circuits has been implemented to interface output data with CMOS family circuit working under the same value voltage of power battery.

VCCO can be then chosen in a voltage range from 2.5 V up to 3.6 volts.

2.2 Serial interface

Communication with the configuration register is done through a serial interface (SRI).
Just after the power on action a message must be transmitted via the serial interface to the TDA9964/52 internal registers to set a correct working configuration.

A writing sequence of a serial message is made of 10 (12) data bit + 4 address bit.
A3,A2,A1,A0,(D11,D10),D9,D8,…,D2,D1; with A3 first bit sent.

The enable not SEN must go low during a low period of the clock CLK but SEN must be go back to 1 only during the high stable state of the clock period.
Be careful, at least one SCLK cycle is needed after the SEN return to 1 in order to latch the data and address to the internal registers.

2.3 Internal registers

The configuration register is programmed to fix the requested conditions by application to the following parameters and functions:

- AGC gain control;
- OFD output control;
- ADC clamp reference control.
- Active edges control for SHP, SHD ,CLAMP's, PBK and CLK.

Timing and how to define the active polarity of all these signals, rising or falling edge, is given in detail in TDA9964/52 specification and can be summarized in the following tables.

2.3.1 OFD function

Serial address A3A2A1A0= 0001

Dec	hex	Typical Value of OFD out
0	00	0.0V
255	ff	1.0 V

2.3.2 AGC gain control

Serial address A3A2A1A0 = 0000. Bit 9 = 0

hex	-4.5dB +Gain	Bit B	bit A	bit 9	bit 8	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0	dec
00	0 dB	x	x	x	x	0	0	0	0	0	0	0	0	0
40	6 dB	x	x	x	x	0	1	0	0	0	0	0	0	64
80	12 dB	x	x	x	x	1	0	0	0	0	0	0	0	128
C0	18 dB	x	x	x	x	1	1	0	0	0	0	0	0	192
FF	24 dB	x	x	x	x	1	1	1	1	1	1	1	1	255

2.3.3 Polarity settings or control pulses

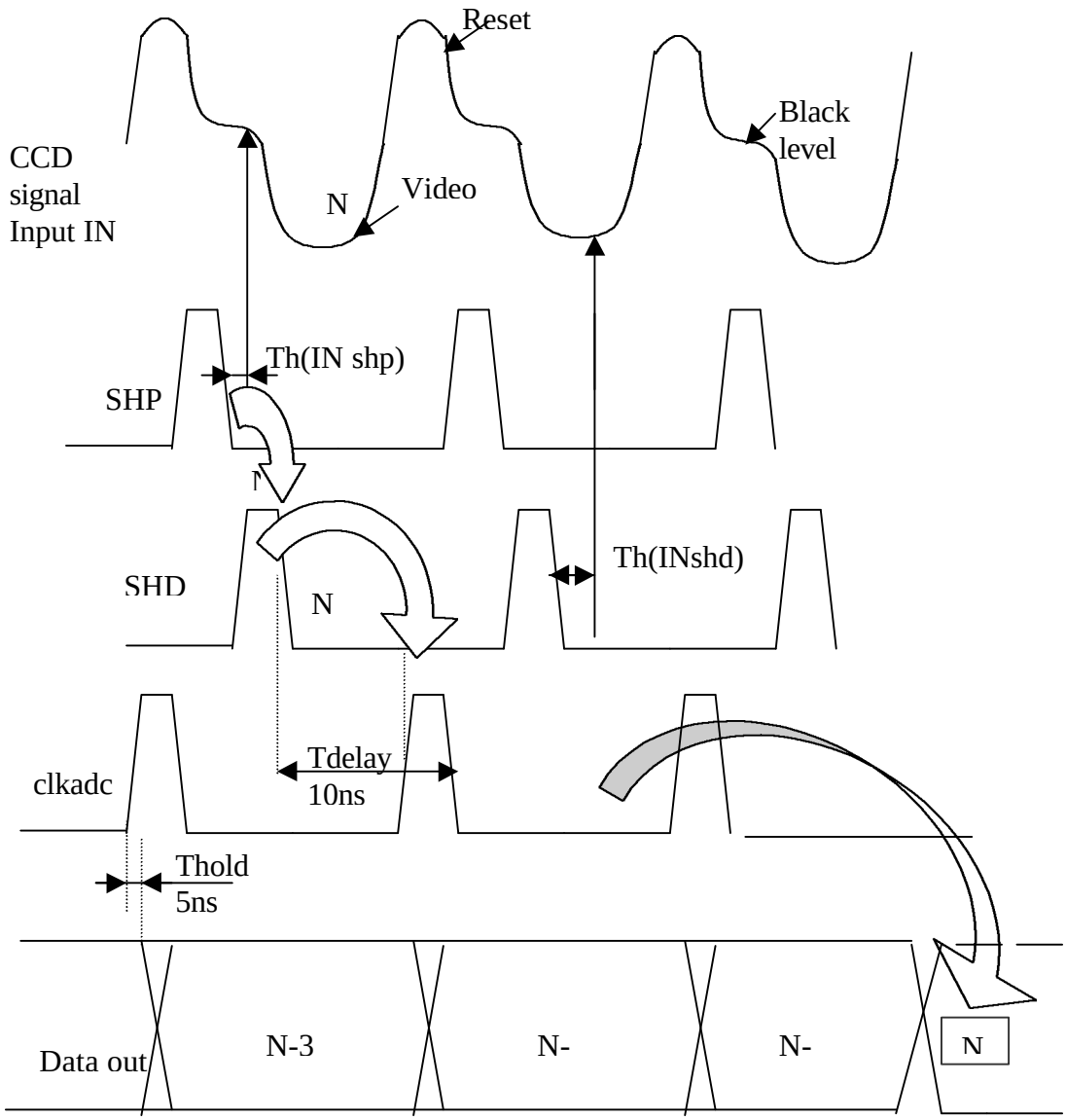
Serial address A3A2A1A0 = 0011; SD2 SD6 SD7 SD9 = 1111

SD4 =1	SHP, SHD active level HIGH
SD5=1	CLK active edge RISING
SD0=1	CLPDM active level LOW
SD1=1	CLOPB active level HIGH
SD3=1	BLK active level HIGH
SD8=0	VSYNC active edge RISING

3 TIMING DIAGRAM

A typical input signal of CCD on the pins IN(p,d) is depicted in fig. 3 as it can be seen on an oscilloscope in comparison the pulses SHP, SHD signals.
The CCD signal can be divided into three main parts, the cross talk with the reset gate pulse, the reset hold level and the actual video level.

Figure 1 - Timing diagram



Inside the TDA9964/52 there is a pipeline delay between the external SHP and SHD signals present at the inputs and the actual internal switch action which sample the CCD signal. This delay is lower than 1 ns.
This delay has to be taken into account during the definition of an application diagram to make sure that the video signal is correctly processed and that no overlap exists between the different sampled periods (black and active video) and SHP, SHD pulse commands.

3.1 CDS function

With video information, reset noise, thermal noise 1/f noise generated are present at the CCD output signal.
Since part of low frequencies noises are assumed to be correlated both during the active part of the video and during the feed through, major part of this noise can be cancelled by subtracting the feed through level from the video.

This classical technique known as doubled correlated sampling uses SHP and SHD pulses to command the internal process of CDS.

At the end the result of this operation in the CDS is the generation of new signal which is now the true useful video level. Then this one will be presented at the input of the digitally controlled amplifier ties down by DSP.

3.2 Controlled voltage amplifier

The active video level varies according to the illumination of the scene observed.
In order to ensure that the maximum of the useful dynamic range of the ADC is utilized even under low light conditions the video signal is then amplified, using this programmable gain amplifier loop (PGA).

The amount of gain is adjusted by information resulting of computation in the DSP and transmitted back to the TDA9964/52 amplifier by messages sent with the 3 wires serial interface using a dedicated protocol described in the data sheet of the TDA9964/52.

This amplified signal is then put on the input of a 12(10) bit analog to digital converter, which samples the video information at the clock pixel rate given a raw of 12(10) data but only 10 msb bit are used in our demoboard which are transmitted by a parallel bus to the DSP.

The functional description of the DSP is described in a previous application note and a DSP board used here in this demonstration camera is this DSP reference board.

3.3 Clamps

There are 2 clamps in this TDA9964/52 front end:

- The CLPDM is a command for the input clamp.
  The main purpose of this clamp is to hold in position the CCD signal in the right input working window of the CDS input in such a way that the black level still remains at the same DC voltage.
  This action is normally made during the reading of the dummy pixels of the CCD but with the TDA9964/52 is it also possible to do it during the optical black period (Reference 1 page 15).

- The CLPOB is the second internal clamp, which is able to correct the output offset found after the double correlated sampling stage just before amplification by AGC.
  The command has to be done during the CCD optical black period.
  The reference level for this clamp is also a value fixed by Vref internal reference.

4 FRONT END TYPICAL APPLICATION

The front end circuit TDA9964/52 used with one SAA 81XX of DSP family I.C Philips is the core of a high quality video applications where image sensor, vertical driver, timing generator, micro controller, memories, and DC-DC converter, are the others functions used to build modern CCD video camera as shown in the figure 8 application diagram.

The whole camera is then made up with the following main integrated circuits:

- CCD sensor LZ 2413 for version NTSC LZ2423 for PAL version
- vertical driver (VD) LR36683 replaced within Sharp by LR36685
- pulse pattern generator (PPG) LZ95G55
- front end for analogue processing and digitalization TDA9964/52 (FE),named "preprocessor"
- digital processing and output formatting (DSP) SAA8112
- memory EEPROM PCD8594
- Lvdc for digital output
- Video encoder SAA7102/03

In addition on the schematic it can be found:

- 2 simple small SMPS stages transform the 5 volts power battery voltage into +15volts and –8 volts needed to bias the CCD and vertical driver;
- a transistor buffer stage to interface the CCD with the FE;
- a non inverting amplifier stage to translate the OFDOUT signal of the FE to the FD input of the CCD;
- a push pull stage to transform the OFDX signal of the PPG into a high voltage pulse command added to the OFD on the FD CCD input (shutter function).
- A simple DC level shifter to change 5V in 3V.

A camdemo is made of two different boards:

- an imaging front end also called IFE board;
- A digital board on which are DSP and encoder circuits.

These boards are connected together by a connector in order to be able to mix different configurations of our circuits (TDA8787A+saa8112 or TDA9964/52+saa8112 …).

In a previous application note, AN97037, evaluation board for camera more details can be found about the description of this concept.

This present application has been modified in the front-end part only to become compatible with the TDA9964/52 circuit.
For the people non-familiar with the DSP SAA family reading this previous document will be beneficial to get better understanding of the DSP SAA8112 performance and behavior used in this demonstration camera.

If there is no basic change for the system point of view due to the substitution of the TDA8786 by TDA9964/52 it can be said that the use of new TDA9964/52 circuit improves the global performance of the basic application a more simple connection with the PPG, lower noise, possible choice of the pulse polarity by soft and lower power consumption. And the application needs less external components.

5 POWER AND GROUNDING RECOMMENDATIONS

When designing a printed circuit board for application such as PC camera, surveillance cameras, camcorders a digital still cameras, care should be taken to minimize the noise.
For the front end integrated circuit, the basic rules of printed circuit board design and implementation of analogue components (such as classical operational amplifiers) must be respected, particularly with respect to power and ground connections.

The following additional recommendation is given for the CDS input pin(s) which is (TDA9964/52) / TDA8786) internally connected to the programmable gain amplifier.

The connections between the CCD, the CCD transistor interface and the CDS input should be as short as possible and a ground ring protection around these connections can be beneficial for noise performances.
Separate analogue and digital supplies provide the best solution; if it is not possible to do this on the board then the analogue supply pins must be de-coupled effectively from the digital supply pins. If the same power supply and ground are used for all pins the de-coupling capacitors must be placed as close as possible to the IC package on two separated VCC distribution line.
In a two-ground system, in order to minimize the noise through package and die parasitic, the following recommendations must be implemented:
All the analogue and digital supply pins must be well de-coupled to the analogue ground plane.
Only the ground pins associated to the digital outputs must be de-coupled to the digital ground plane. The analogue and digital ground planes must be connected together at one point as close to the ground pin associated with the digital outputs.
The digital output pins and theirs associated lines should be shield by the digital ground plane which in this case can be used then as return path for digital signal.
Never use a digital ground plane under analogue wires and analogue ground plane under digital connections.

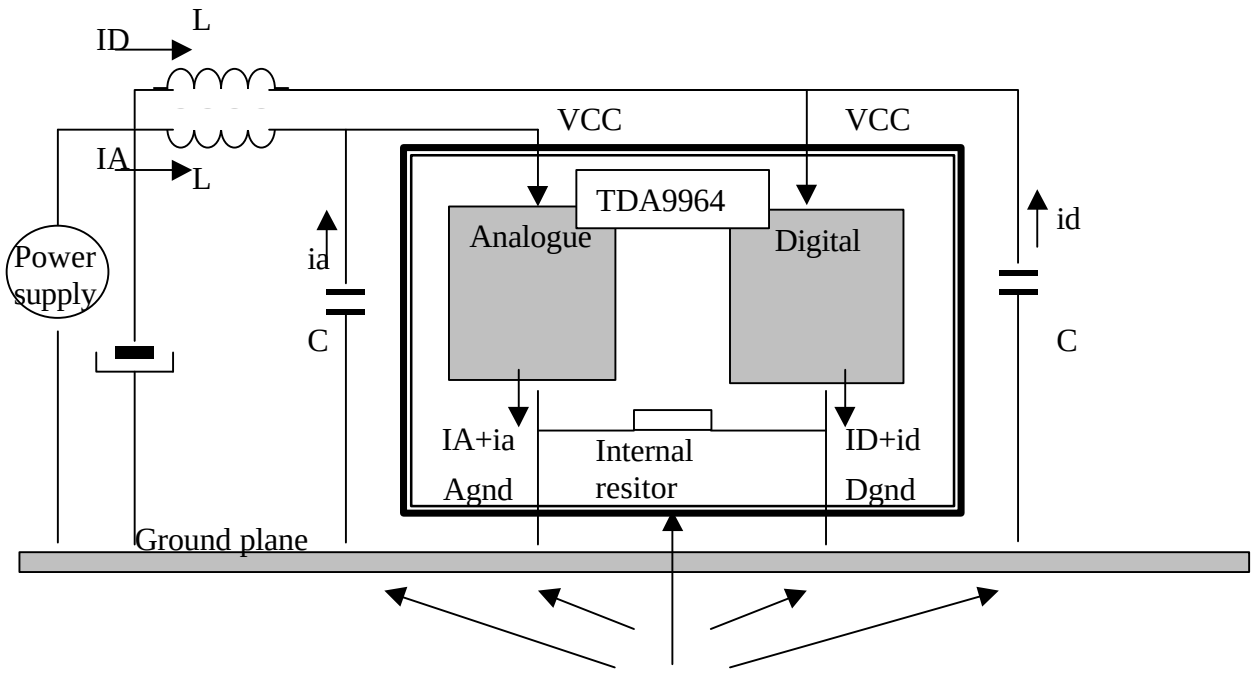


Figure 2 - Grounding connections

On the printed board area loop of supply current and impedance of different ground connections must be minimized, the de-coupling capacitors C (ceramic capacitor) must be placed as close as possible to the VCCA and VCCD pins.

Series inductors in power supply lines may be used to improve de-coupling
(E.g. 1…5 µh or BLM components).

Using above de-coupling scheme, both analogue and digital supply connections can be connected together to a single stable 5 volt supply.

6 INTERFACE CONNECTOR PINING

In the description list below and in the IFE diagram:

J1 = I2C / UART /DSP connector
J2 = 12 bit + service signals output connector for frame grabber

Names on connector **J1**

1	+5 V	2	+5 V
3	GND	4	GND
5	SCLK INPUT	6	SDEN INPUT
7	n.c	8	CLK1
9	CLK2	10	VD
11	SDATA INPUT	12	HD
13	ACLXP PPG internal reset	14	FI PPG Field Index
15	EEUD PPG Electric Exposure 2	16	GND
17	EENR PPG Electric Exposure 3	18	+5 V n.u.
19	SMD1 PPG shutter control 1	20	ACLK
21	NINT PPG Non Interlace Select	22	SMPS Clock for DC-DC power
23	n.c	24	DATA 11
25	DATA 10	26	DATA 9
27	DATA 8	28	+5V n.u.
29	DATA 7	30	GND
31	DATA 5	32	DATA 6
33	DATA 3	34	DATA 4
35	SCLK INPUT	36	DATA 2
37	SDATA INPUT	38	SDEN INPUT
39	STANDBY INPUT	40	DACOUT
41	GND	42	GND
43	+5V	44	5 +V

Rq: SCLK, SDEN and SDATA, inputs to the TDA9964/52 are connected twice on this connector due to the SAA8112 preprocessor bus control hardware designed for 12 bit length register instead of 16 bit in this case so we use 3 other pins from the microcontroller of the SAA8112 and former used in another application.

Names on connector **J2**

1	DATA 0	2	DATA 11
3	DATA 1	4	GND
5	DATA 2	6	DATA 10
7	DATA 3	8	GND
9	DATA 4	10	GND
11	DATA 5	12	GND
13	DATA 6	14	GND
15	DATA 7	16	GND
17	DATA 8	18	GND
19	DATA 9	20	GND
21	HD	22	GND
23	VD	24	FI
25	CLOCK1	26	GND

7 STRAP CONFIGURATION

Few straps allows the user to configure the power supplies and OFD
VCCA , VCCD, VCCO are power supply inputs from preprocessor TDA9964/52

TC1: connect/disconnect OFD (CCD substrate polarization)

TC2: connect/disconnect 3.3v power supply to VCCD's&VCCO

TC5: connect/disconnect 3.3v power supply to VCCA's

TC4: connect/disconnect pin 43 from J1 to VCCD's&VCCO

TC3: connect/disconnect pin 44 from J1 to VCCA's

TC6: connect/disconnect VCCA's to VCCD's&VCCO

8 ELECTRICAL DIAGRAMS

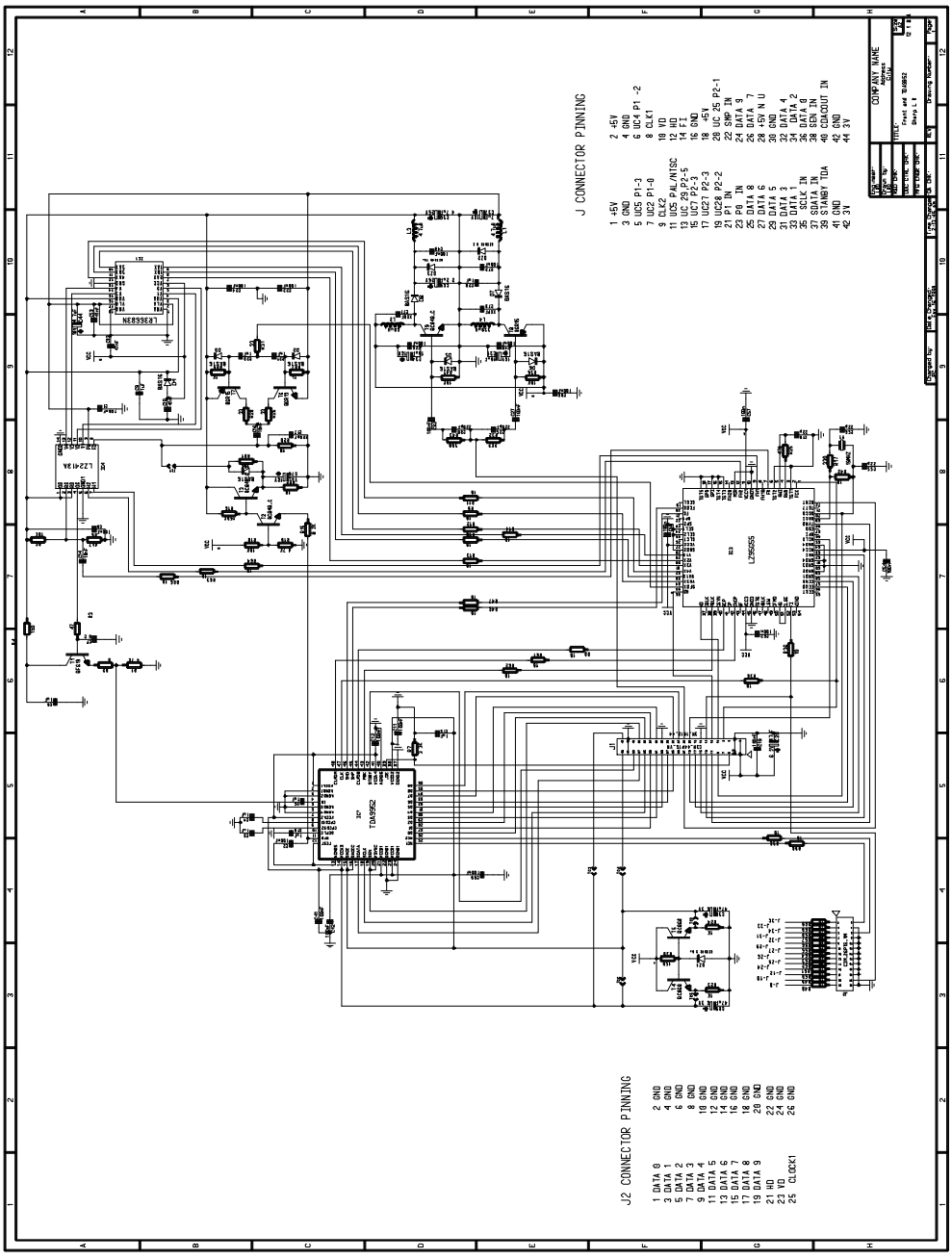


Figure 3 – Electrical schematic

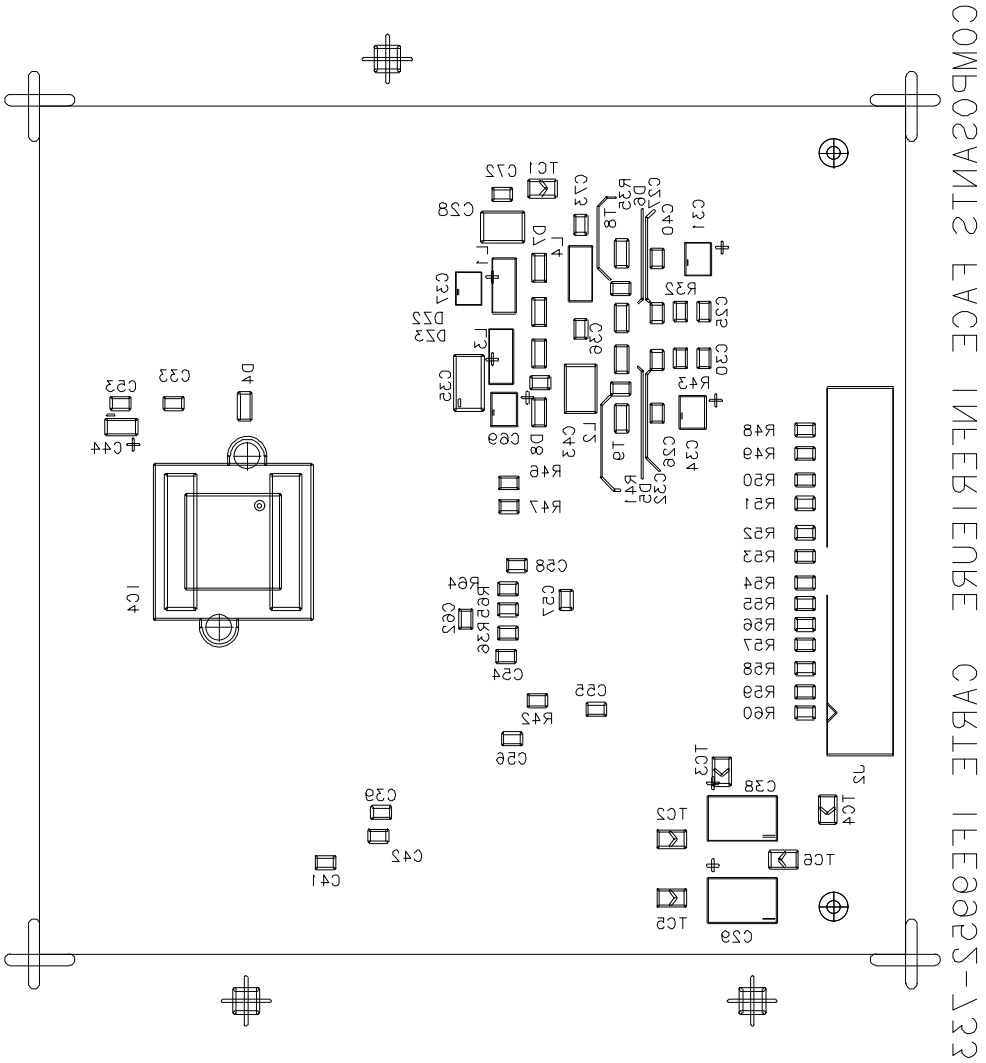


Figure 4 – component implementation lower side

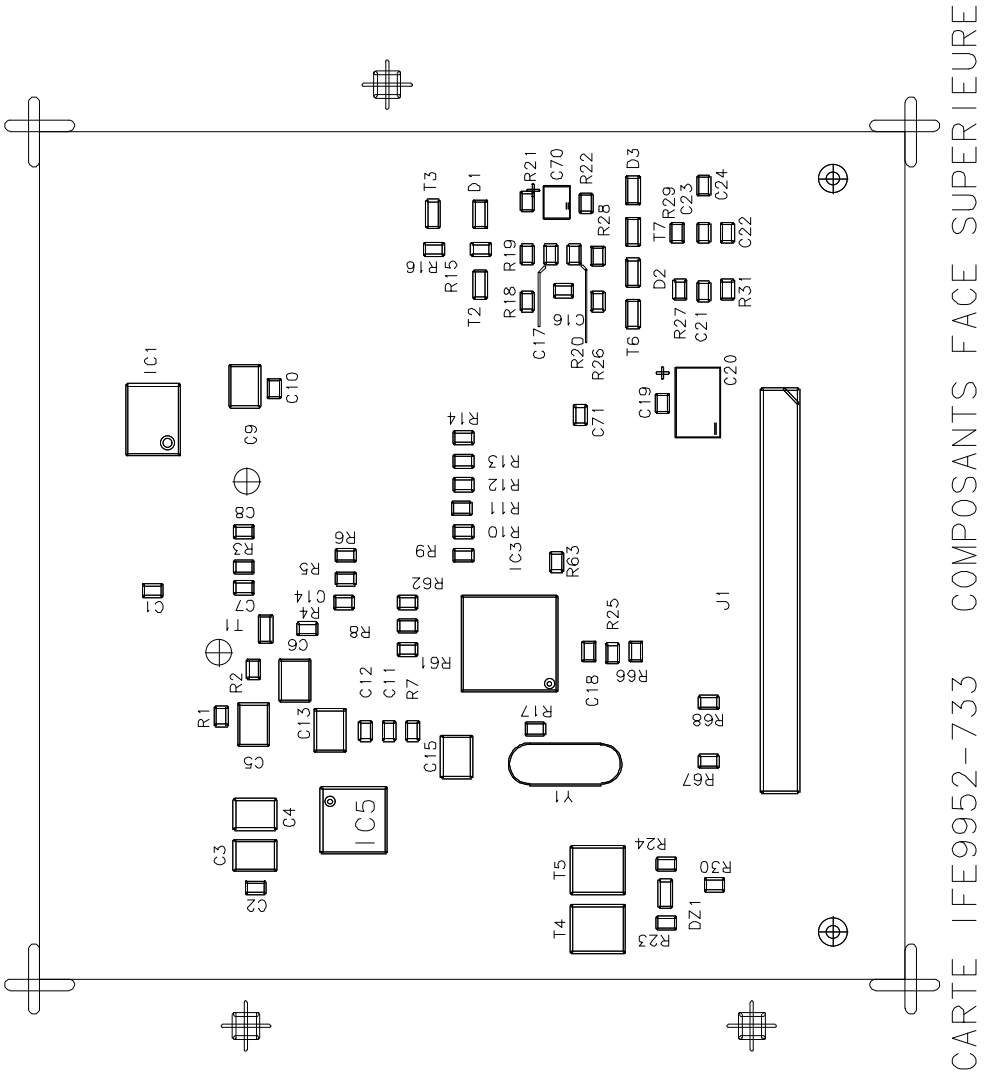


Figure 5 – component implementation upper side

9 OPTOMECHANIC BLOCK

In front of the TDA9964/52 there is a CCD sharp LZ2413 which is a ¼ type solid state image sensor having 542*498 pixels. This CCD is compatible with the NTSC standard. For a Pal application this CCD can be changed and directly replaced by the LZ2423 CCD type but in this case the quartz oscillator must be also be changed:

- 19.06993 MHz is used for NTSC version;
- 19.3125 MHz is used for PAL camera;

and in the same time the declaration of the type NTSC or PAL option must be swap in the setting of the DSP program and all parameters concerning the actives and black Windows pixels must be updated this can be done by help of the graphic interface user GUI developed in our US lab to demonstrated the SAA 8112 possibilities. See Ref 2.

In the front of the CCD there is a optical low pass filter from American KSS, Inc. This particular filter is currently being produced by this manufacturer under the reference OG-BF389 (3122 168 7514.0), the size of this infrared filter is 7.75*7.25*3.27 mm and must be introduced in the optical block as shown below.

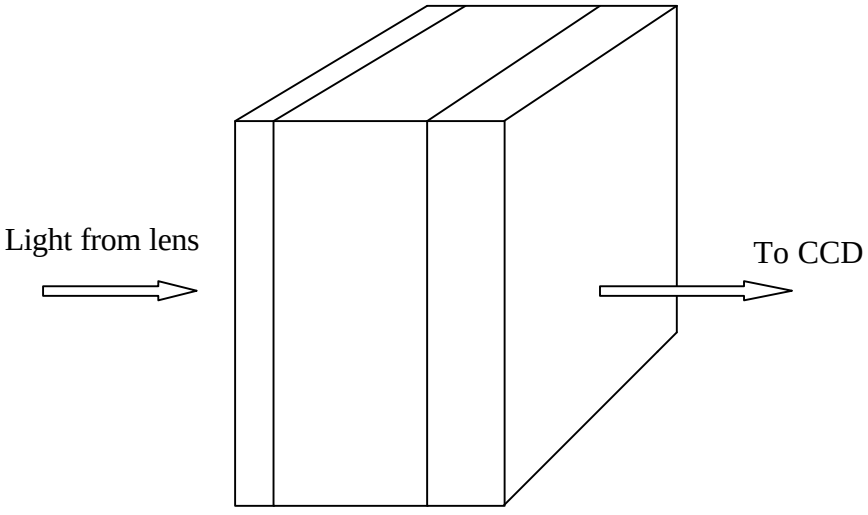


Figure 6 – Optical filter

In addition each kit is containing the following elements:

- 1 piece CS mount interface (Fig m1);
- 1 piece under-plate (fig m2);
- 1 piece CS mount ring (fig m3);
- 1 piece retaining ring (fig m4);
- 1 piece filter foan (fig m 5);
- 2 screws M2.5.

The IFE kit can be delivered with CS CCTV lens coming from different suppliers.

Lens which generally are 4mm F 1.2 or 8 mm F1.2 depending available material on stock.

9.1 Optical support drawings

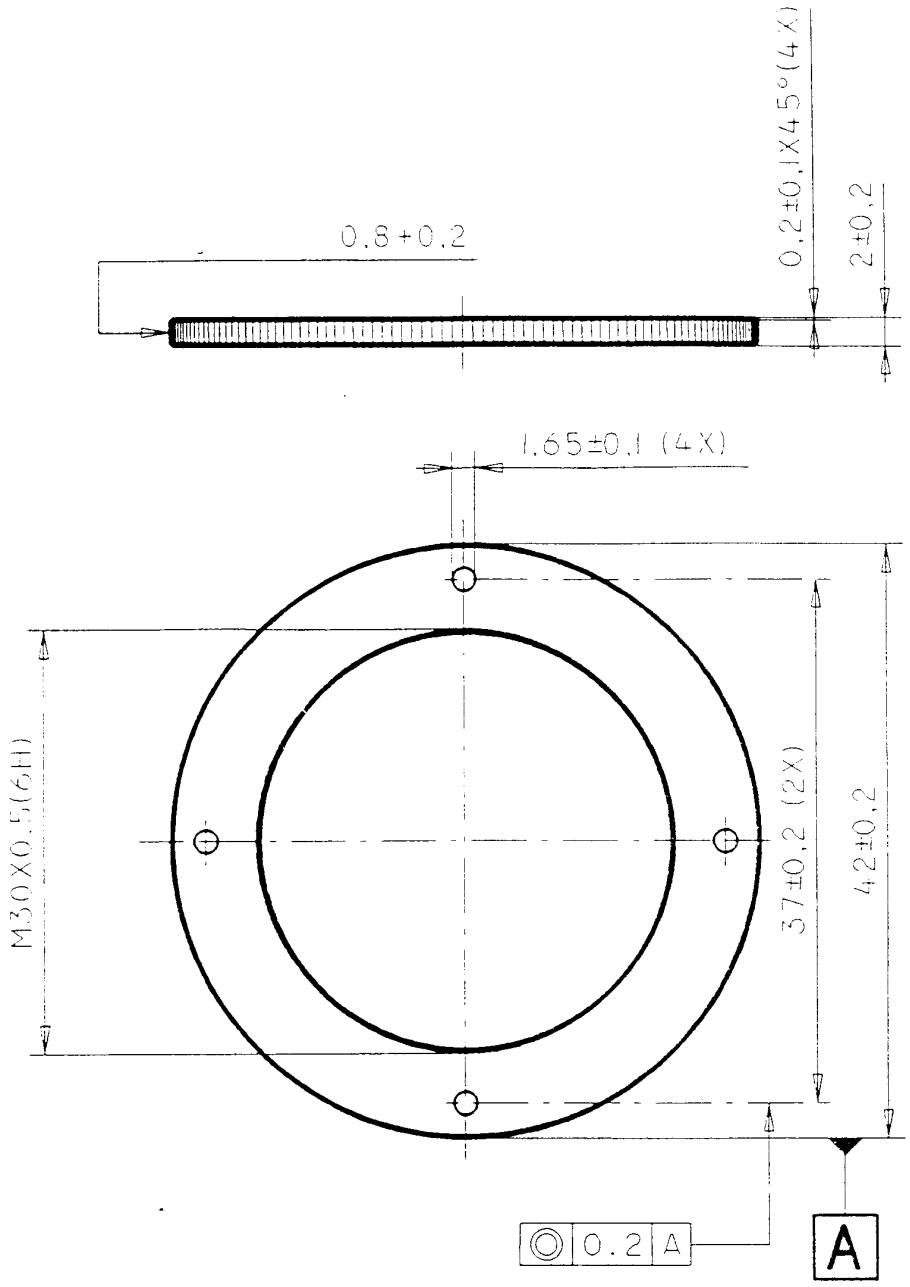


Figure 7 – Retaining ring

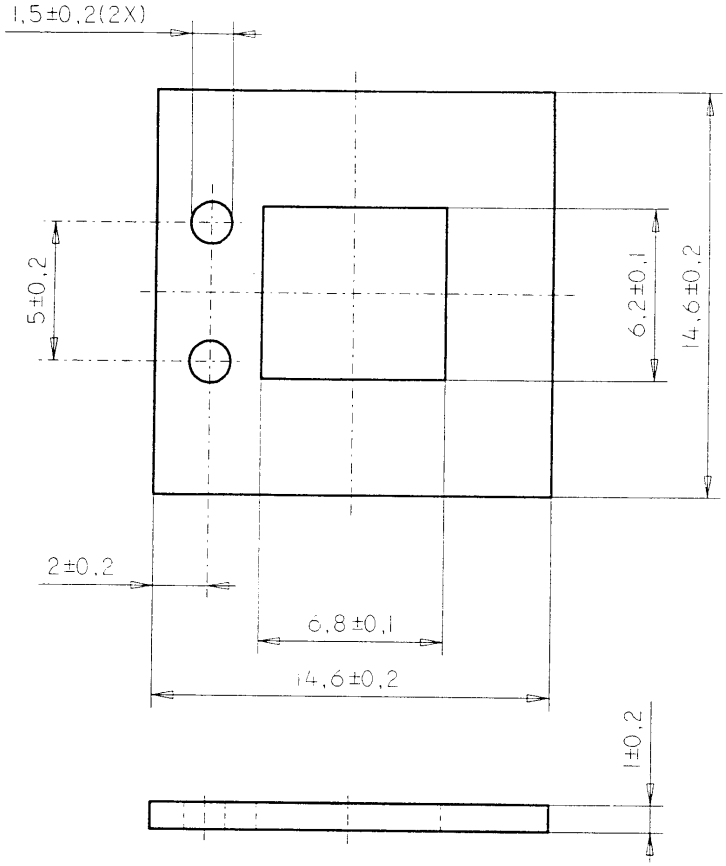


Figure 8 – Filter foan

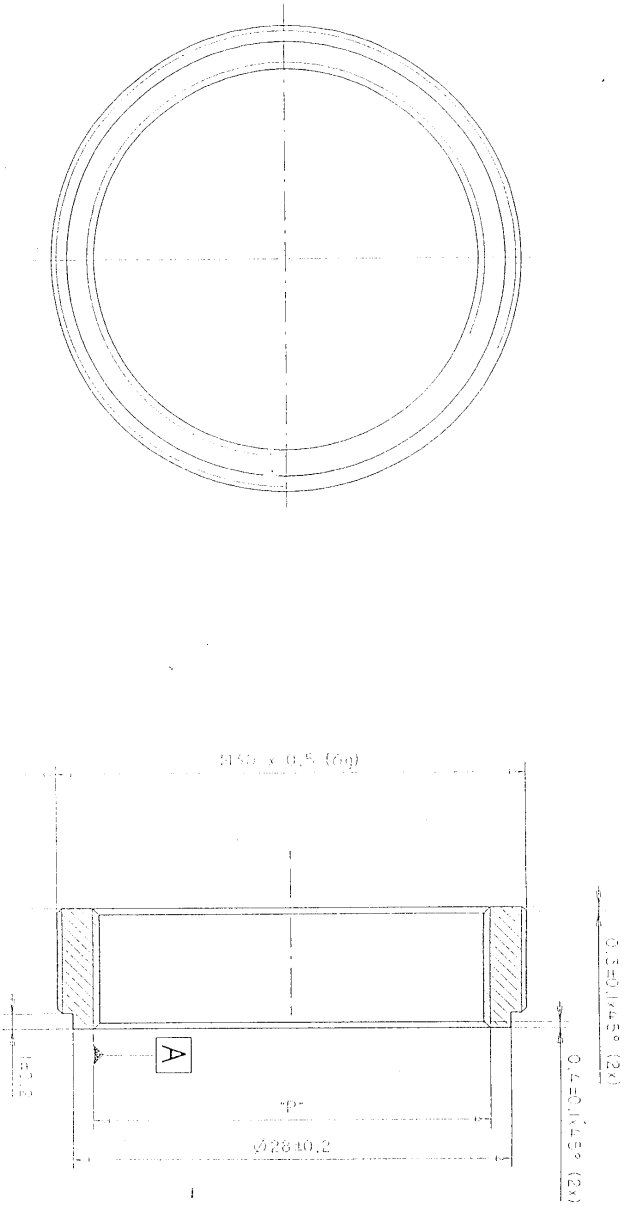


Figure 9 – CS inout interface

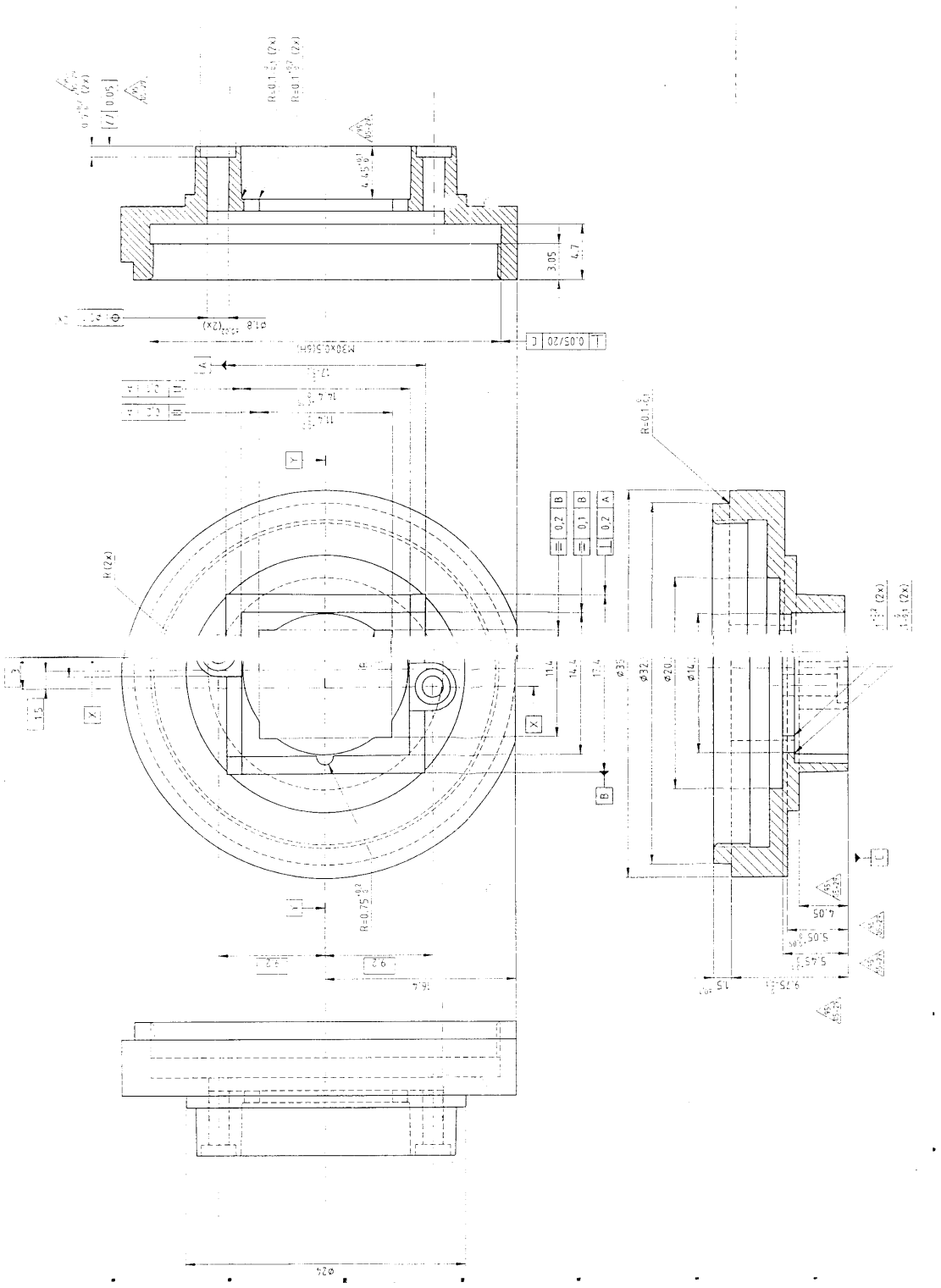


Figure 10 – CS inout ring

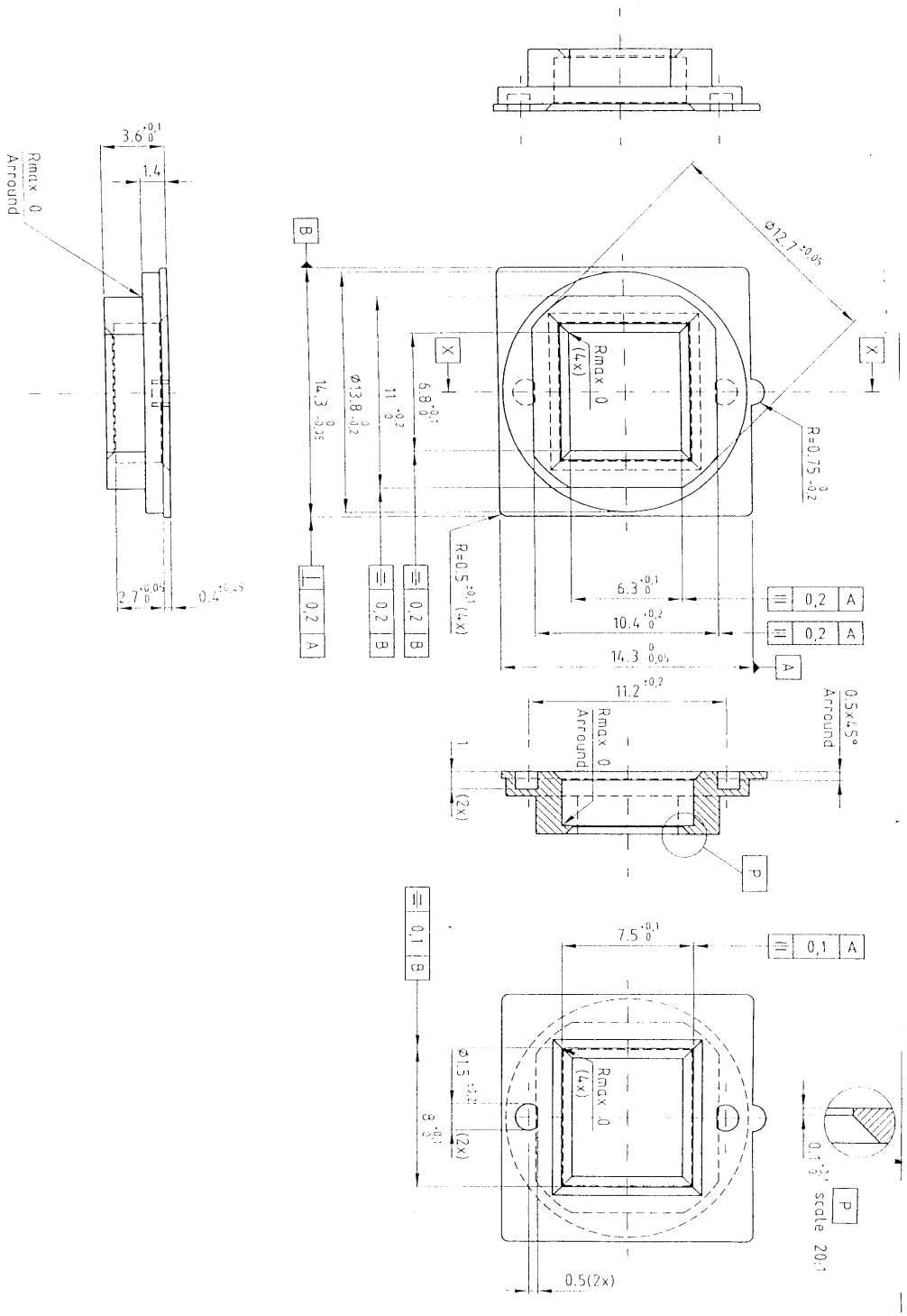


Figure 11 – Retaining filter

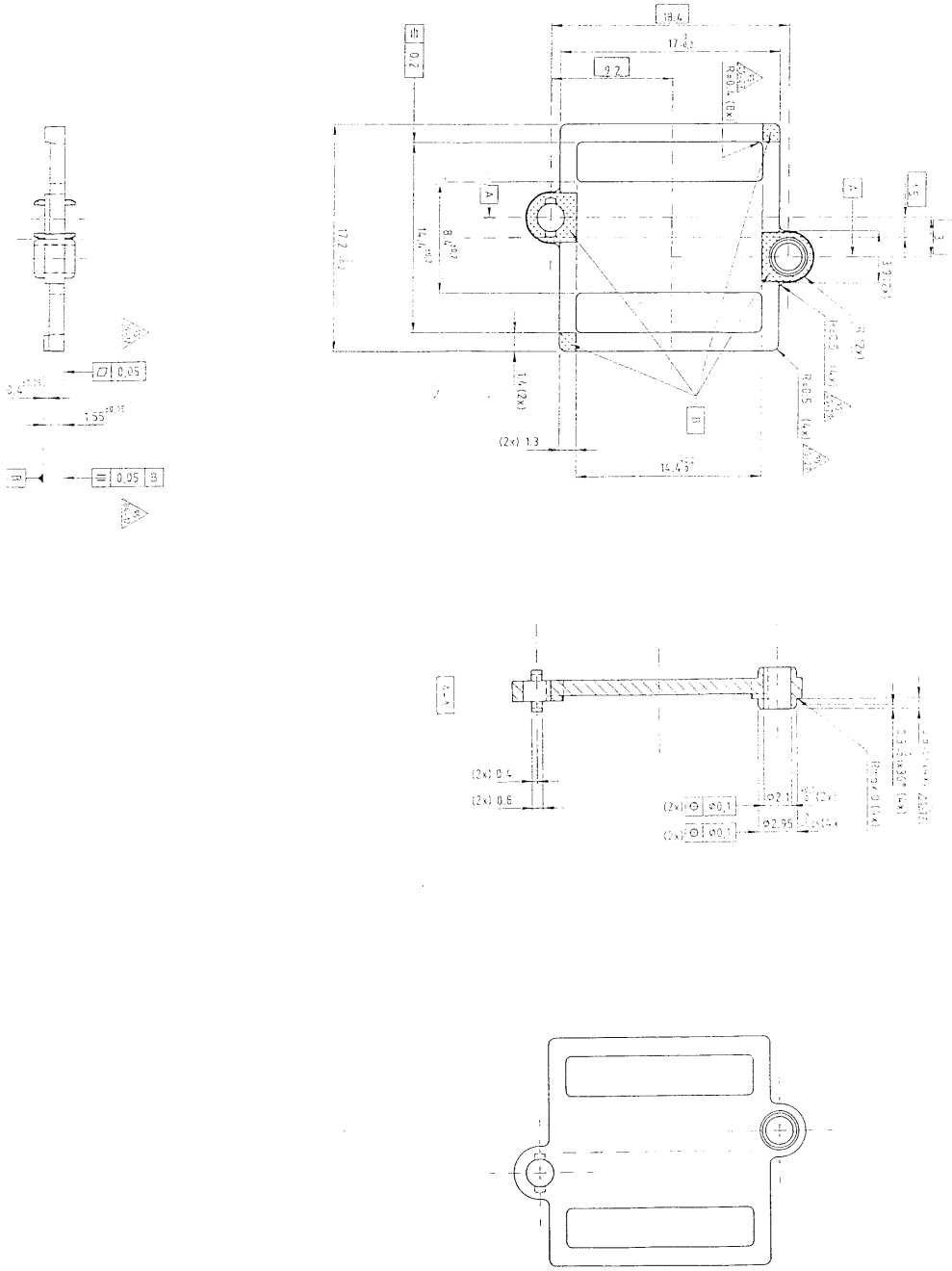


Figure 12 – Under plate

10 ANNEXES

Specifications	LZ2413A
Specifications	LZ95G55
Specifications	LR36683
Specifications	TDA9964/52

11 REFERENCES

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Author: Jürgen Krehnke

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Authors: S. Jacquet, R. Morisson

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(Modification of V3.11 for TDA8786 by C. Kohler and H. Jacquemin) .

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